STP5950

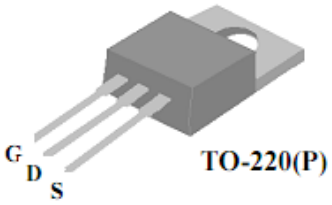
P Channel Enhancement Mode MOSFET

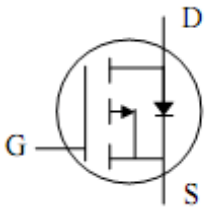
-35.0A

DESCRIPTION

STP5950 is the P-Channel logic enhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology.
This high density process is especially tailored to minimize on-state resistance.
These device is particularly suited for low voltage application, notebook computer power management and other battery circuits where high-side switching.

PIN CONFIGURATION





FEATURE

- -100V/-15A, $R_{DS(ON)}$ = 36mΩ (Typ.) @V_{GS} = -10V
- -100V/-10A, $R_{DS(ON)}$ = 40mΩ @V_{GS} = -4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- TO-220 package design

ABSOULTE MAXIMUM RATINGS (Ta = 25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		VDSS	-100	V
Gate-Source Voltage		VGSS	±20	V
Continuous Drain Current (TJ=150℃)	TA=25℃ TA=80℃	ID	-35.0 -33.0	A
Pulsed Drain Current		IDM	-140	A
Power Dissipation	TA=25℃	PD	140	W
Operation Junction Temperature		TJ	-55/150	℃
Storgae Temperature Range		TSTG	-55/150	℃
Thermal Resistance-Junction to Ambient		RθJA	62	℃/W

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ELECTRICAL CHARACTERISTICS (Ta = 25℃ Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,ID=-250mA	-100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},ID=-250uA	-1.0		-2.5	V
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-100V,V_{GS}=0V			-1	uA
		V_{DS}=-80V,V_{GS}=0V T_J=85℃			-10	
Drain-source On-Resistance	$R_{DS(on)}$	V_{GS}=-10V,I_D=-15A V_{GS}=-4.5V,I_D=-10A		36 40	45 55	mΩ
Forward Transconductance	gfs	V_{DS}=-30V,I_D=-10A		21		S
Diode Forward Voltage	V_{SD}	I_S=-1A,V_{GS}=0V			-1.0	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=-50V V_{GS}=-10V I_D≡-10A		95	150	nC
Gate-Source Charge	Q_{gs}			16	30	
Gate-Drain Charge	Q_{gd}			13.8	26	
Input Capacitance	C_{iss}	V_{DS} =-25V V_{GS}=0V F=1MHz		2800	3600	pF
Output Capacitance	C_{oss}			1300	1700	
Reverse TransferCapacitance	C_{rss}			320	420	
Turn-On Time	$t_{d(on)}$	V_{DS}=-50V R_G= 25Ω I_D=-5A		58	110	nS
	tr			24	50	
Turn-Off Time	$t_{d(off)}$			215	450	
	tf			55	100	

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TYPICALCHARACTERICTICS

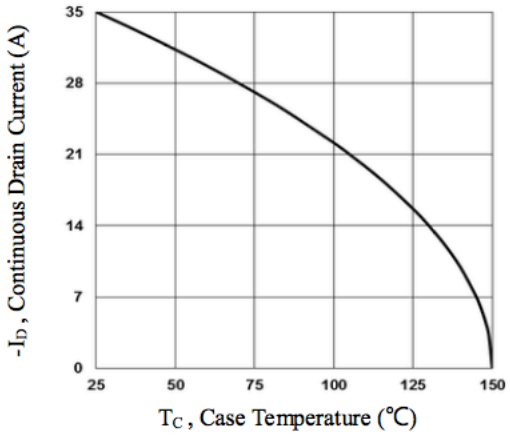

Fig.1 Continuous Drain Current vs. T_C

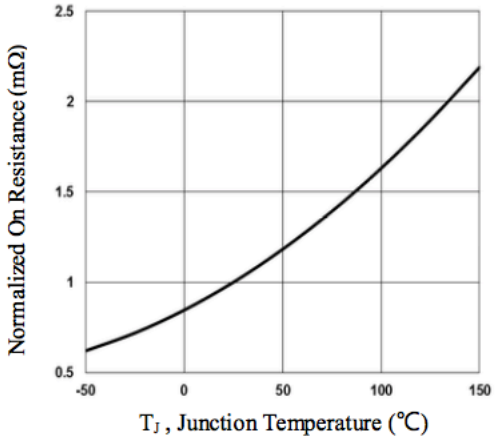

Fig.2 Normalized RDSON vs. T_J

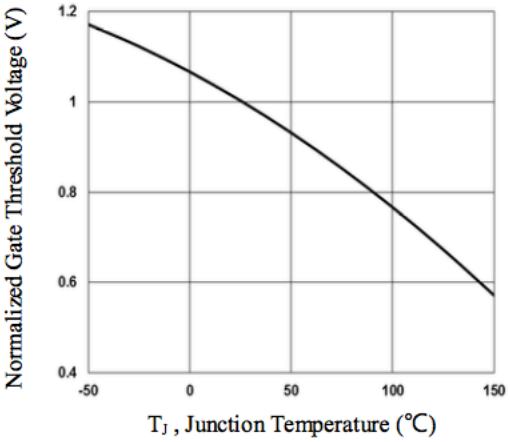

Fig.3 Normalized V_{th} vs. T_J

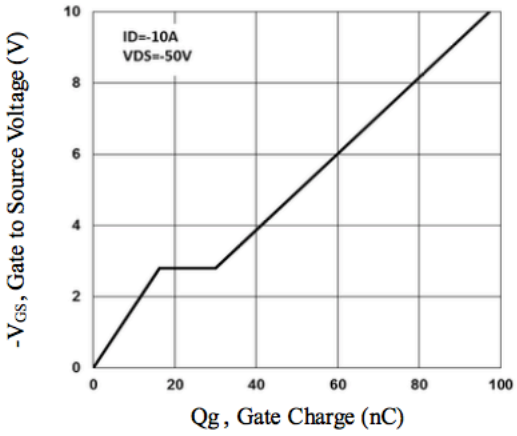

Fig.4 Gate Charge Waveform

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TYPICAL CHARACTERICTICS

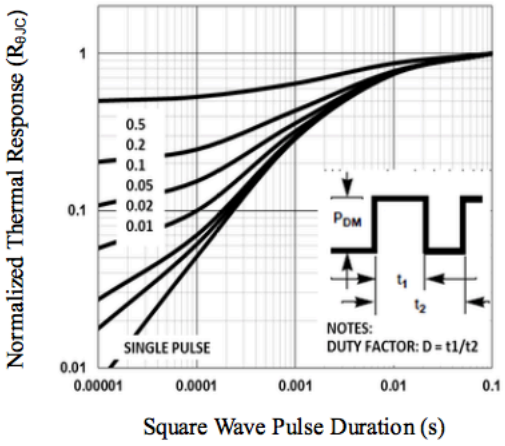

Fig.5 Normalized Transient Impedance

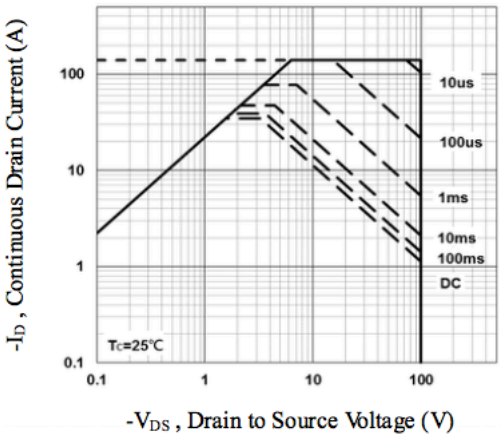

Fig.6 Maximum Safe Operation Area

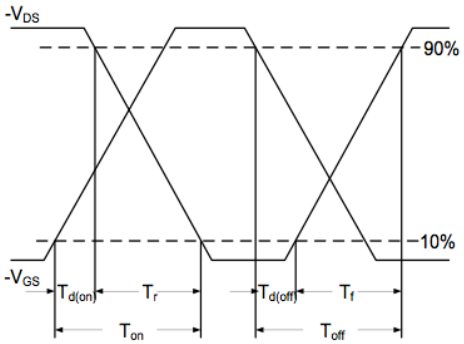

Fig.7 Switching Time Waveform

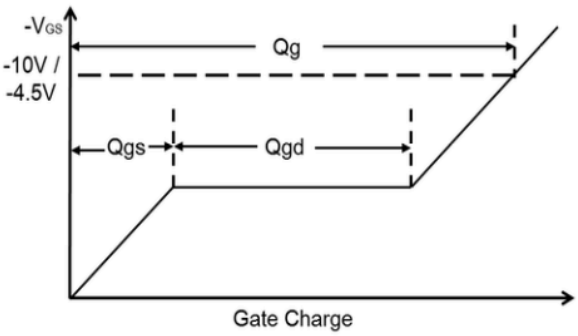

Fig.8 Gate Charge Waveform

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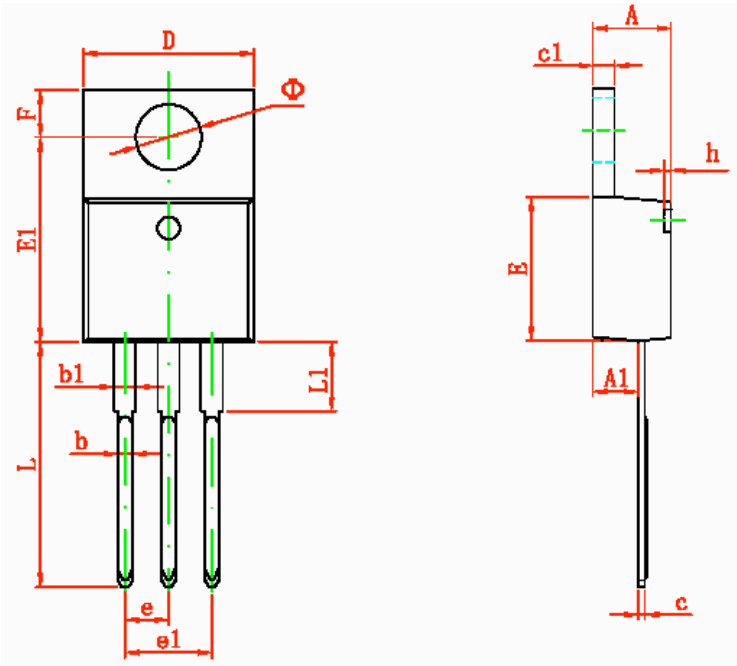
TO-220-3L PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.470	4.670	0.176	0.184
A1	2.520	2.820	0.099	0.111
b	0.710	0.910	0.028	0.036
b1	1.170	1.370	0.046	0.054
c	0.310	0.530	0.012	0.021
c1	1.170	1.370	0.046	0.054
D	10.010	10.310	0.394	0.406
E	8.500	8.900	0.335	0.350
E1	12.060	12.460	0.475	0.491
e	2.540 TYP		0.100 TYP	
e1	4.980	5.180	0.196	0.204
F	2.590	2.890	0.102	0.114
h	0.000	0.300	0.000	0.012
L	13.400	13.800	0.528	0.543
L1	3.560	3.960	0.140	0.156
Φ	3.735	3.935	0.147	0.155

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